Remarks

Entry of the amendments, reconsideration of the application, as amended, and allowance of all pending claims are respectfully requested. After entry of the amendments, claims 1-18 are pending.

With the above amendments to independent claims 1 and 7, applicant is clarifying the claimed language without acquiescing to any rejection. Further, dependent claims 13-18 are being added to more particularly point out and distinctly claim various features of applicant's claimed invention. Support for the amendments can be found throughout the specification. As examples, support for claim 13 can be found in paragraphs 27 and 28 of applicant's specification, as well as in FIG. 2; support for claim 14 can be found in paragraphs 24 and 30; support for claim 15 can be found in paragraph 33; support for claim 16 can be found in paragraph 30; support for claim 17 can be found in paragraphs 34 and 35; and support for claim 18 can be found in paragraph 24. Thus, no new matter is being added.

In the Office Action dated February 20, 2004, claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the term "substantially" is said to create an ambiguity. In an effort to advance prosecution of this application and without acquiescing to the rejection, applicant has amended claim 7 to remove the term substantially. Therefore, applicant respectfully requests withdrawal of the §112 rejection.

Further, claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al. (U.S. Patent No. 5,784,393). Applicant respectfully, but most strenuously, traverses this rejection to any extent deemed applicable to the amended claims.

In one aspect, applicant's invention is directed to error detection and correction of system-wide errors on interconnecting address, data and control lines. Single or multiple bit errors in various components of a data processing system, including those arising in interfaces, such as non-integrated intermittent interconnections, are able to be detected and corrected. To accomplish this, parity bits are generated in one portion of the data processing system, such as a sending portion, and the parity bits are tested in a second portion, such as the receiving portion,

to detect one or more errors. The one or more errors are then corrected in the second portion. This allows intermittent errors occurring with, for instance, solder connections, mating connector pins or other types of mechanical connections to be detected and corrected.

In one particular aspect, applicant claims a method of providing error detection and correction in an interface between two portions of a data processing system. The method includes, for instance, generating, in a first portion of the data processing system, parity bits corresponding to a plurality of bits of the interface; transmitting across the interface the parity bits together with the plurality of bits of the interface; testing, in a second portion of the data processing system, that the parity bits correspond to the plurality of bits for which parity was encoded; and detecting and correcting, in the second portion of the data processing system, one or more errors in the plurality of bits for which parity was encoded. Thus, in this aspect of applicant's claimed invention, applicant detects and then corrects errors. This is very different from the teachings of Byers et al.

While Byers teaches error detection, Byers does not teach error correction. The many details provided in Byers are concerned with and describe error detection and not error correction. This is clear by the fact that error correction is not described in any of the 20 figures. Instead, Byers goes into great detail describing error detection and just mentions that when an error is detected, it is presented to the user (Col. 8, lines 60-62). There is absolutely no teaching of how to correct an error in Byers.

In one instance, Byers mentions an error correction block 874; however, applicant respectfully submits that this appears to be a typographical error, since that same block is referred to earlier in that paragraph and in the drawings as an error detection logic block. Nevertheless, regardless of what the block is called, Byers still does not teach how to correct an error. Byers merely states that the block will provide the faulty read address for further processing (Col. 22, lines 15-25). When read in context, Byers describes that this processing is simply an indication of whether the fault was caused by a soft error or a hard error. If it is a soft error, then the contents may be reloaded. If it is a hard error, then the computer system is interrupted. There is absolutely no description of how the error itself would be corrected. Since Byers fails to describe error correction, applicant respectfully submits that Byers does not teach

applicant's claimed invention that specifically recites detecting and correcting one or more errors. For at least this reason, applicant respectfully requests withdrawal of the rejection based on Byers.

Also, applicant's claimed invention further recites that the error correction is performed in a second portion of a data processing system, while the generating of parity bits is performed in a first portion. This is very different from the teachings of Byers. If Byers was to teach error correction, it would teach that it is to be performed in the same portion as the generating, i.e., the transmitting portion. Byers goes to great lengths to describe how all the error detection should be performed by only the transmitting user. For example, Byers states:

> A transmitting user may provide a data word and a number of corresponding parity bits to the bus via the output buffer. However, unlike the prior art fault detection schemes, the receiving user may not be capable of regenerating the parity bits and performing the compare function as described above. In the exemplary embodiment, the data word and the number of parity bits may be provided back into the transmitting user, via the input buffers of the transmitting user, wherein a parity check may be performed by the transmitting user. (Col. 4, lines 13-23)

Thus, if Byers was to describe error correction, it would teach that error correction would be performed in the same portion of the system, i.e., the transmitting portion, as the parity generation and error checking. One certainly would not be motivated by the teachings of Byers to have the parity generation separate from the error detection and correction.

Based on the foregoing, applicant respectfully submits that independent claim 1, as well as independent claim 7, are patentable over Byers. Further, the dependent claims are patentable for the same reasons as the independent claims, as well as for their own additional features.

For example, dependent claim 13 explicitly recites that the parity generation is performed in the sending portion of the system and the error detection and correction are performed in the receiving portion. This is very different from the teachings of Byers in which there is no description of error correction, and even if there was error correction, it would follow that it would be performed in the sending portion, since Byers teaches over and over that fault detection

should be constrained to only the sending portion. Thus, Byers does not teach or suggest this aspect of applicant's claimed invention.

As a further example, dependent claims 2 and 8 recite that the interface is a non-integrated intermittent interconnection. This is very different from the bus of Byers that is an integrated assembly. Thus, Byers does not teach or suggest this aspect of applicant's claimed invention.

As another example, dependent claims 3 and 9 indicate that the plurality of bits for which parity was encoded include data, address and control signals. Thus, errors are detected and corrected for control signals, as well as for data and address lines. This is not taught or suggested in Byers. While Byers mentions control signals for various applications, Byers does not teach or suggest that errors arising from control signals are to be detected and corrected using parity bits. Byers is silent as to this. Thus, Byers does not teach or suggest this aspect of applicant's claimed invention.

As yet a further example, applicant recites that the detecting and correcting of errors are performed asynchronously (e.g., dependent claim 15). That is, the detection and correction of one or more errors are not reliant on clock cycles. This is contrary to Byers that teaches that the detecting of errors is reliant on multiple clock signals.

As yet a further example, applicant recites in dependent claims 16 and 17 that the correcting comprises reconstructing one or more bits using the transmitted bits of the interface and that the reconstruction is regardless of the nature of the error, respectively. Again, Byers does not teach the correction of errors, and in particular, Byers does not teach a particular error correction scheme, such as reconstructing bits using transmitted bits of the interface. Byers is silent as to this. Thus, Byers does not teach or suggest this aspect of applicant's claimed invention.

As a further example, applicant recites detecting and correcting multiple bit errors (e.g., dependent claim 18). Again, this is in contrast to Byers which can only detect and correct one error at a time. There is no provision in Byers for detecting and correcting multiple bit errors.

For all of the above reasons, applicant respectfully requests an indication of allowability for all claims pending herein.

Should the Examiner wish to discuss this case with applicant's attorney, please contact applicant's attorney at the below listed number.

Respectfully submitted,

Blanche E. Schiller

Blanche E. Schiller
Attorney for Applicants
Registration No.: 35,670

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HESLIN ROTHENBERG FARLEY & MESITI P.C.
5 Columbia Circle
Albany, New York 12203-5160
Telephone: (518) 452-5600
Facsimile: (518) 452-5579